MGX-445040-S5 4.4 – 5.0 GHz, 10 W GaN-on-SiC Power Amplifier

Description

The MGX-445040-S5 is a packaged single-stage C-band GaN-on-SiC linear power amplifier delivering 40 dBm (10 W) of saturated power with 13.0 dB of small signal gain. It can be used as a final stage PA for portable radio applications including MANET or UAVs, or a high-power driver for 5G NR cellular infrastructure.

RF ports are nominally matched to 50 Ω for ease of use, with integrated DC blocking capacitors at RF input and output.

The active device is fabricated using a state-of-the-art GaN-on-SiC process and packaged in a small form factor, 5 x 5 mm thermally enhanced plastic air-cavity QFN.



5 x 5 mm AQFN-32L Package

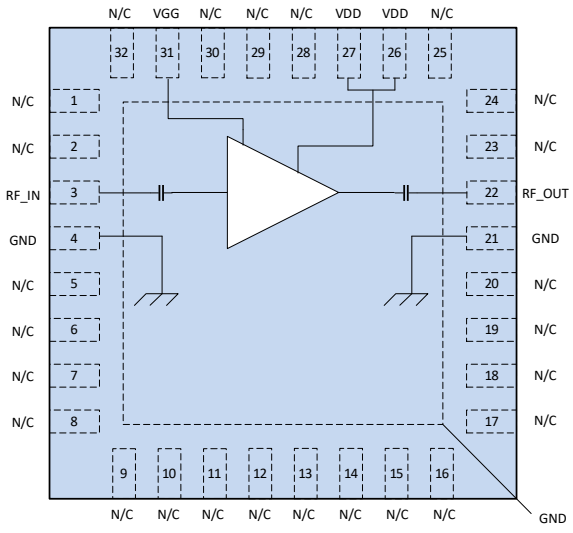
Applications

- MANET (Portable Ad-hoc NETwork)
- UAV datalink
- 5G NR cellular infrastructure (n79 band)

Product Features

- Frequency range 4.4 - 5 GHz
- Saturated output power 40 dBm
- Small signal gain 13.0 dB
- RF ports matched to 50 Ω and DC blocked
- Power added efficiency 55 % @ P3dB
- DC bias 56 mA @ +28 V

Block Diagram



Ordering Information

Part Number	Description
MGX-445040-S5	Tape and Reel
MGX-445040-S5EV	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+32 dBm
Device Voltage (Vd)	+28 V
Power Dissipation (Pdiss)	20 W (Tc = 85 °C)
Junction Temperature (Tjmax)	225 °C (MTTF >1 x 10^6 hours)
Storage Temperature	-40 to +125 °C

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	3.6 °C / W (Tc = 85 °C)

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	4.4		5	GHz
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vd)			28	V
Gate Voltage (Vg)	-4.5	-2.35	-2.2	V
Quiescent Current (Idq)		56		mA
Power down Voltage (Vg)		-3		V

The device is tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution



High-performance RF integrated circuits are highly sensitive to electrostatic discharge (ESD) and may contain unprotected inputs and outputs. Handling and assembly should be conducted in an ESD-controlled environment. It is recommended that ESD precautions and protocols are adopted to minimise the risk of electrostatic discharge and protect product integrity.

Electrical Specification

Results taken on the MGX-445040-S5EV, where board losses have been de-embedded using TRL calibration.

Vd = 28 V, Idq = 56 mA, Ta = +25 °C and Zo = 50 Ω (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		4.4		5	GHz
Small Signal Gain	4.4 GHz 4.7 GHz 5 GHz		13 13.5 13.5		dB
Reverse Isolation	4.4 GHz to 5 GHz		-27		dB
Psat (P3dB)	4.4 GHz 4.7 GHz 5 GHz		40		dBm
PAE	At saturated Pout, 4.7 GHz		55		%
OIP3	Average. Pout = 33 dBm / tone. At 4.7 GHz. Tone Spacing = 20 MHz		45		dBm
ACPR	Avg. Pout = 32 dBm, at 4.7 GHz 256-QAM, RRC = 0.1, PAPR ~ 7.8 dB Symbol Rate = 16.8 Ms/s		35		dBc
EVM	Avg. Pout = 32 dBm, at 4.7 GHz 256-QAM, RRC = 0.1, PAPR ~ 7.8 dB Symbol Rate = 16.8 Ms/s		3		%
Input Return Loss	4.4 GHz to 5 GHz		10		dB
Output Return Loss	4.4 GHz to 5 GHz		10		dB
Gate Voltage (Vg)	Idq = 56 mA, No RF Input		-2.4		V
Standby Current (Id)	Vg = -4.5 V, No RF Input		100		µA
Drain Current (Id)	At Psat, 4.7 GHz		670		mA
Gate Current (Ig)	Idq = 56 mA, Vd = 28 V		20		µA

Pin Assignments

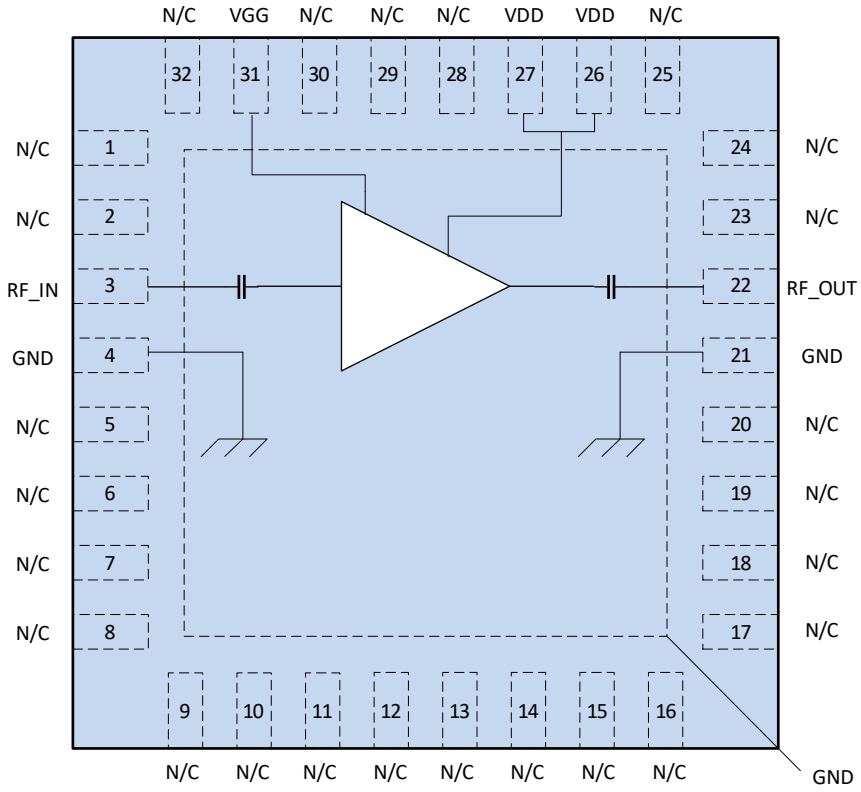


Figure 1 - Top View

Table 1 - Pin Assignments

Pin	Name	Description
3	RF_IN	RF input, nominally 50 Ω with integrated DC-blocking capacitor.
4, 21	GND	DC and RF Ground
1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 23, 24, 25, 28, 29, 30, 32	N/C	No connection (or connect to GND)
22	RF_OUT	RF output, nominally 50 Ω with integrated DC-blocking capacitor.
26, 27	VDD	Drain voltage
31	VGG	Gate voltage
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

The bottom exposed die pad must be connected to the ground plane on the board for electrical and thermal reasons, so a good connection is critical. Attention should be paid to the solder paste design to ensure that there isn't too much solder on the ground area thus causing the device to float and resulting in poor placement of part. See later section with recommended land pattern.

Typical Performance

The following plots show typical performance characteristics of MGX-445040-S5 measured on the evaluation board (Part Number MGX-445040-S5EV). Board losses have been de-embedded from the measurement results using TRL calibration.

Test conditions unless otherwise noted

Vd = 28 V, Idq = 56 mA, Ta = 25 °C (unless stated otherwise) and Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10 %.

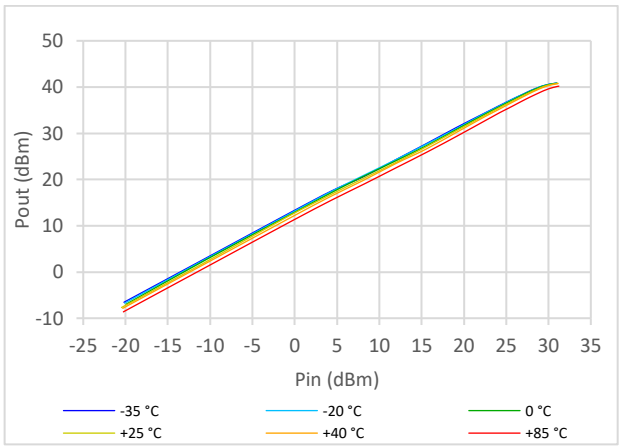


Figure 2 - Pout vs Pin at 4.4 GHz

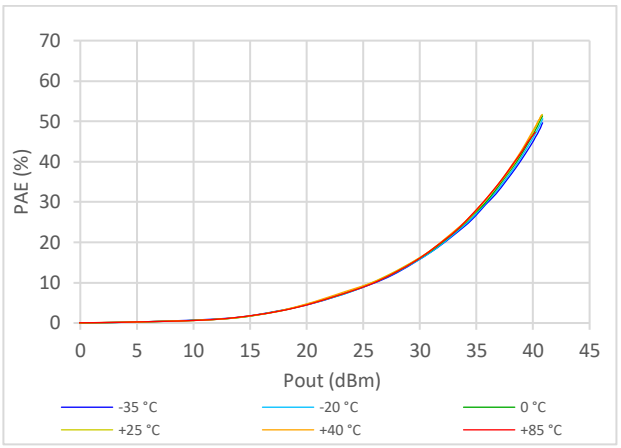


Figure 3 - PAE vs Pout at 4.4 GHz

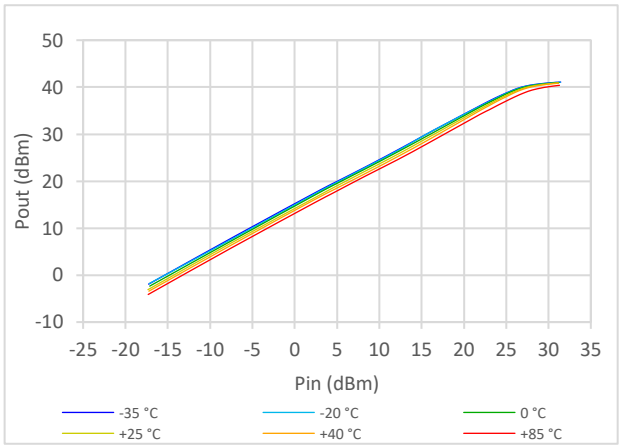


Figure 4 - Pout vs Pin at 4.7 GHz

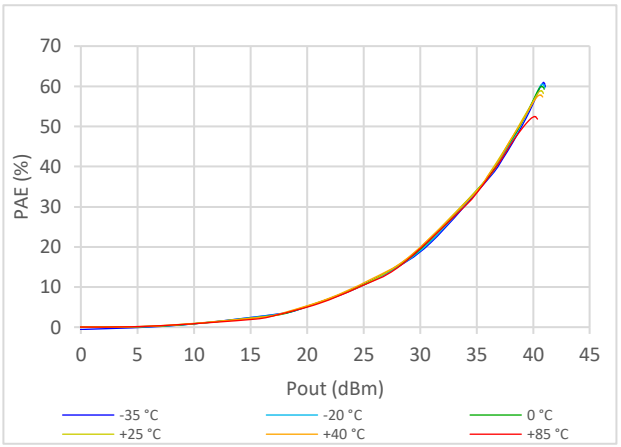


Figure 5 - PAE vs Pout at 4.7 GHz

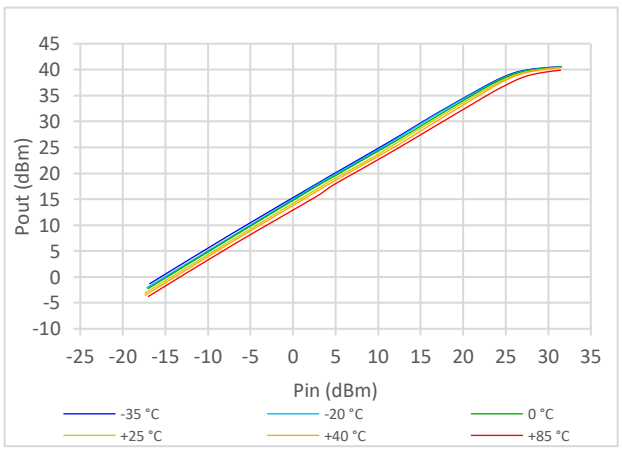


Figure 6 - Pout vs Pin at 5.0 GHz

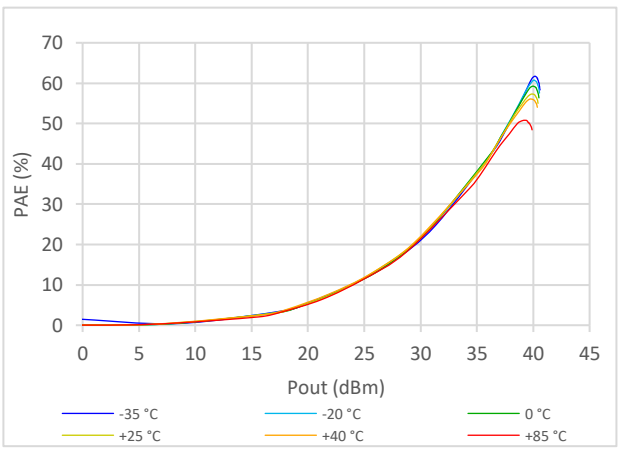


Figure 7 - PAE vs Pout at 5.0 GHz

Test conditions unless otherwise noted

Vd = 28 V, Idq = 56 mA, Ta = 25 °C (unless stated otherwise), Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10 %.

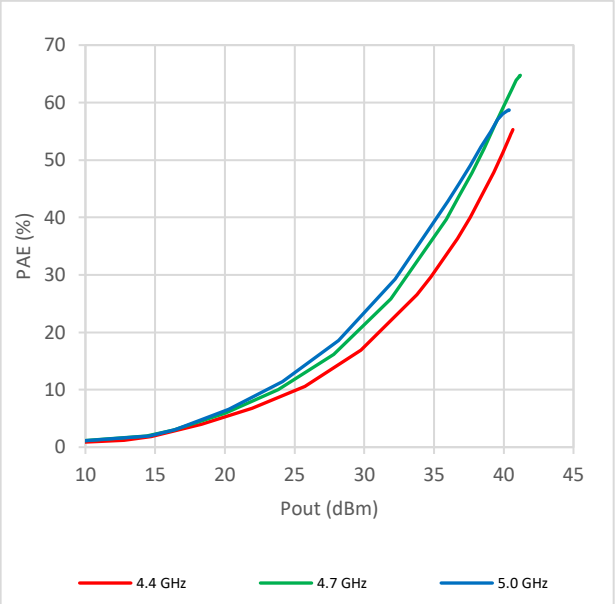


Figure 8 - PAE vs Pout

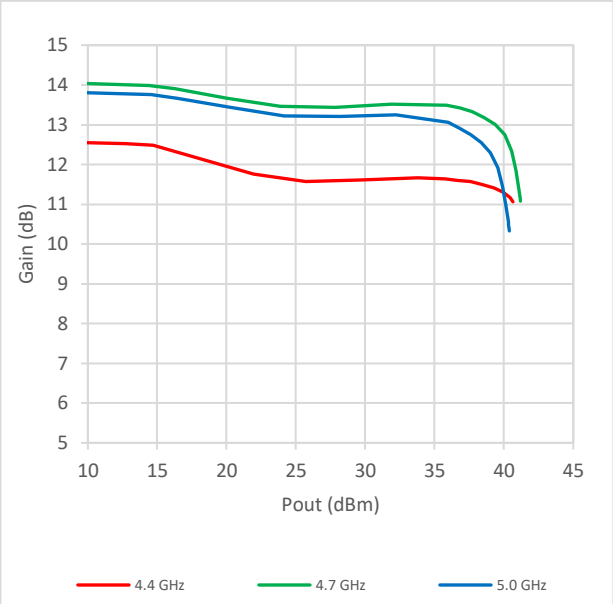


Figure 9 - Gain vs Pout

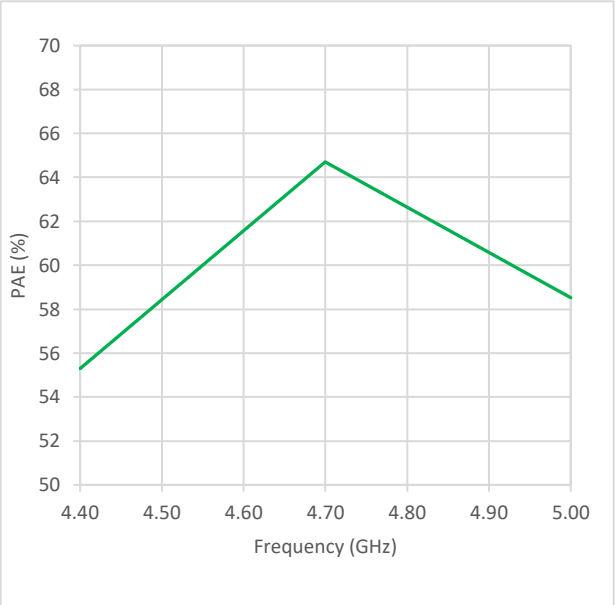


Figure 10 - PAE @P3dB vs Frequency

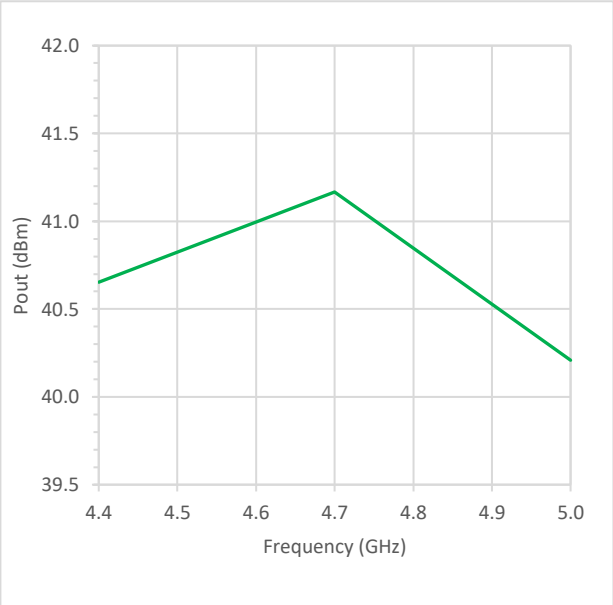


Figure 11 - Pout @P3dB vs Frequency

Test conditions unless otherwise noted

Vd = 28 V, Idq = 56 mA, Ta = 25 °C (unless stated otherwise), Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10 %.

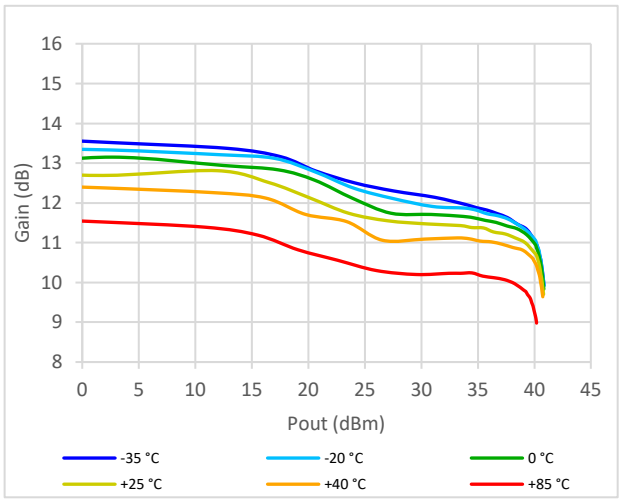


Figure 12 - Gain vs Pout at 4.4 GHz

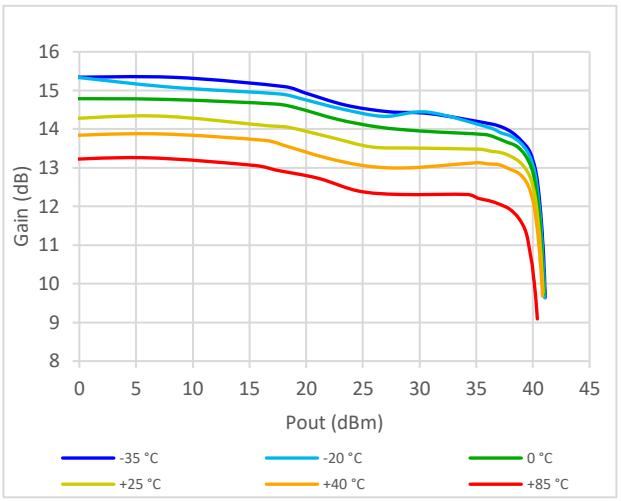


Figure 13 - Gain vs Pout at 4.7 GHz

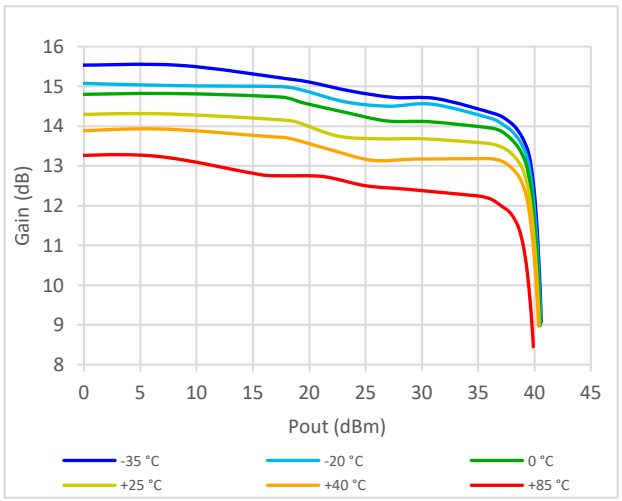


Figure 14 - Gain vs Pout at 5.0 GHz

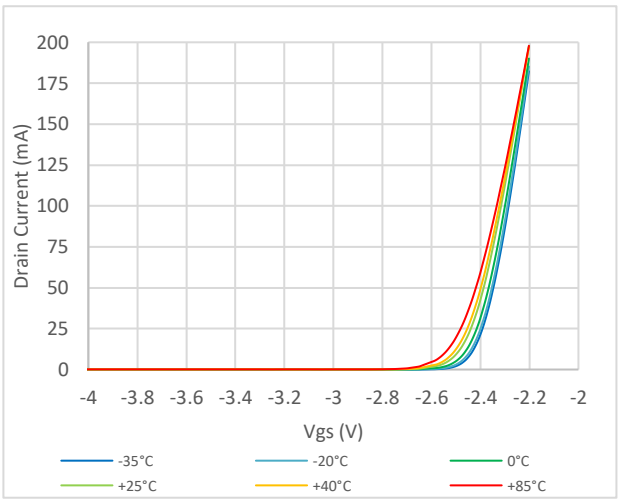


Figure 15 - Ids vs Vgs

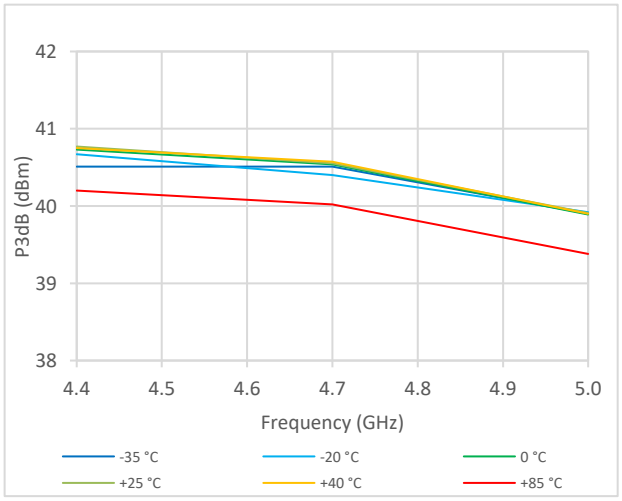


Figure 16 - Pout @ P3dB vs Frequency

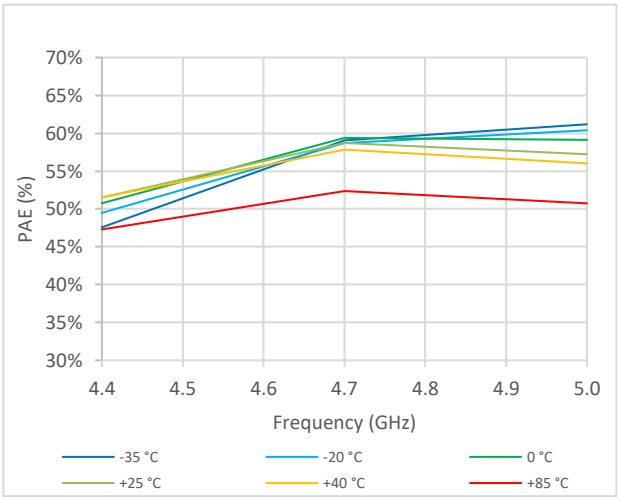


Figure 17 - PAE @ P3dB vs Frequency

Test conditions unless otherwise noted

Vd = 28 V, Idq = 56 mA, Ta = 25 °C, Zo = 50 Ω. 256-QAM, RRC- 0.1, Symbol rate – 16.8 Ms/s, PAPR ~7.8 dB (CCDF – 0.01%)

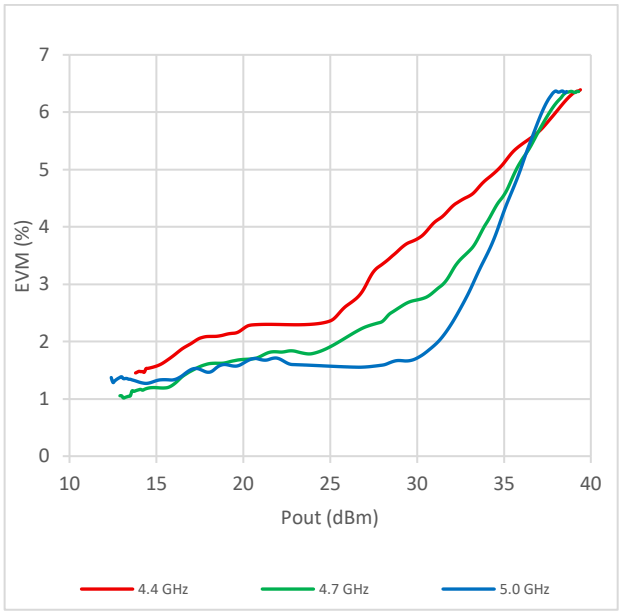


Figure 18 - EVM vs Pout

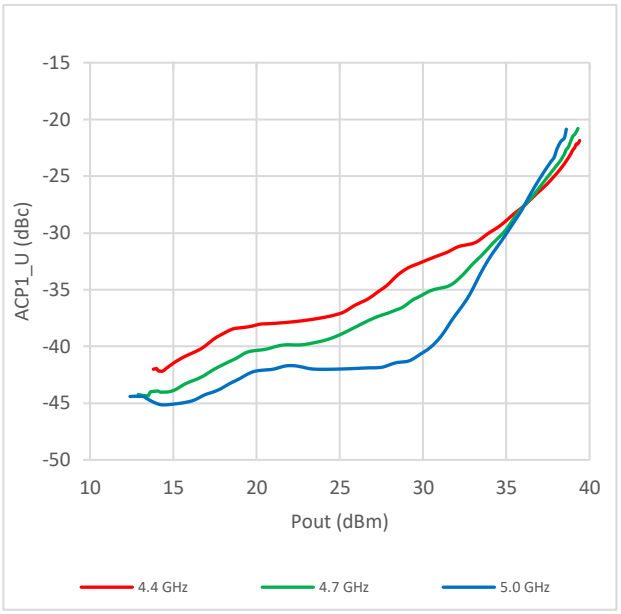


Figure 19 - ACP1_U vs Pout

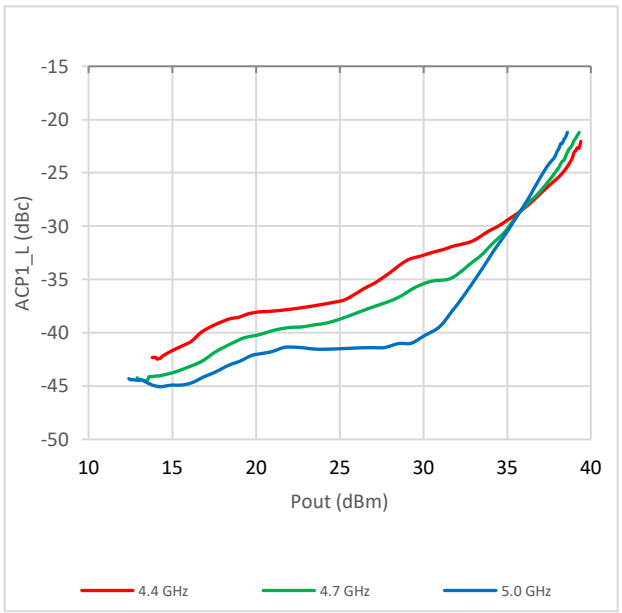


Figure 20 - ACP1_L vs Pout

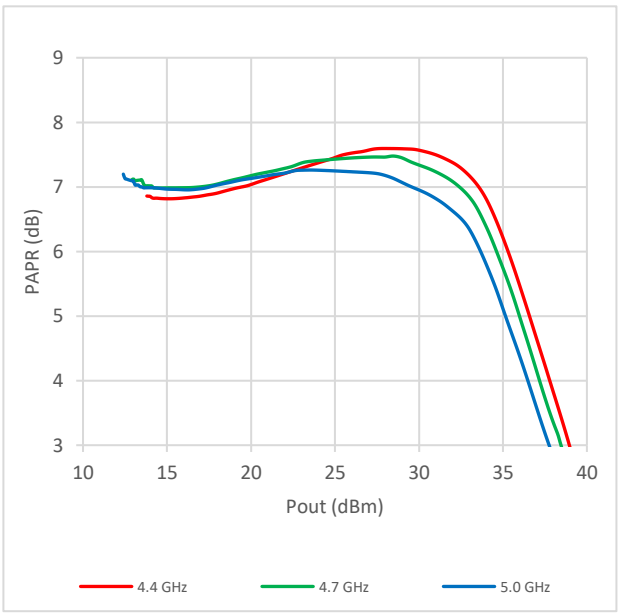


Figure 21 - PAPR vs Pout

Test conditions unless otherwise noted

Vd = 28 V, Ids = 56 mA, Ta = 25 °C, Zo = 50 Ω. Two-tone input with 20 MHz spacing.

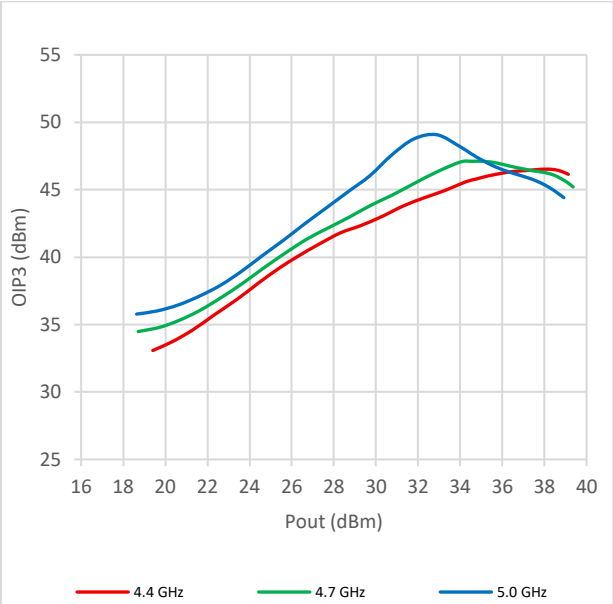


Figure 22 - OIP3 vs Pout

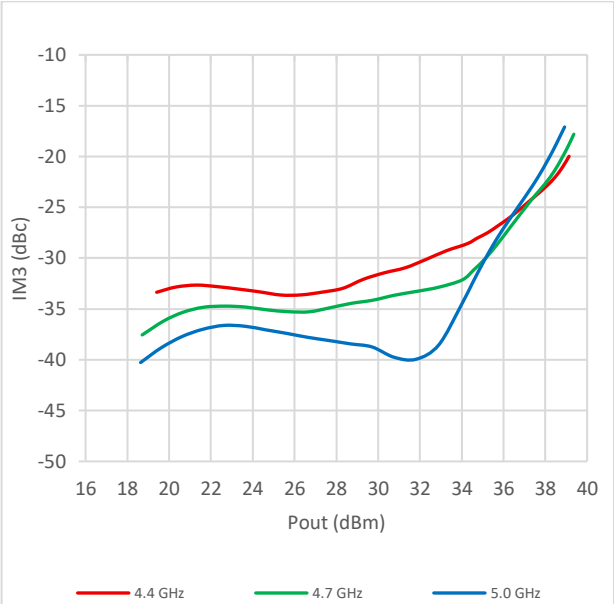


Figure 23 - IMD3 vs Pout

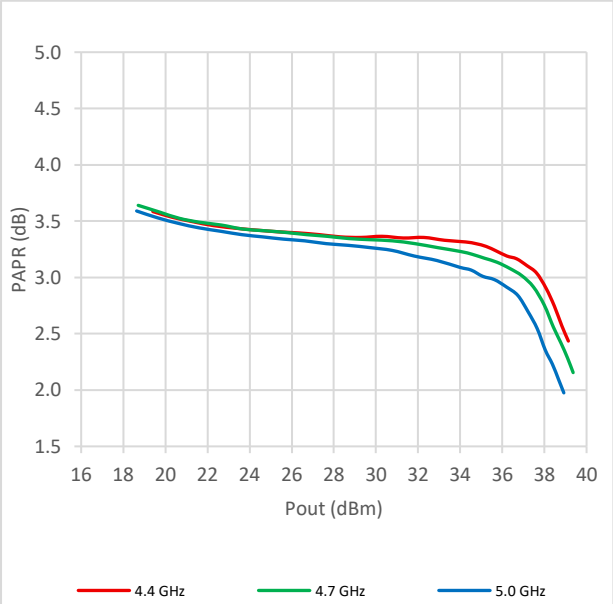


Figure 24 - PAPR vs Pout

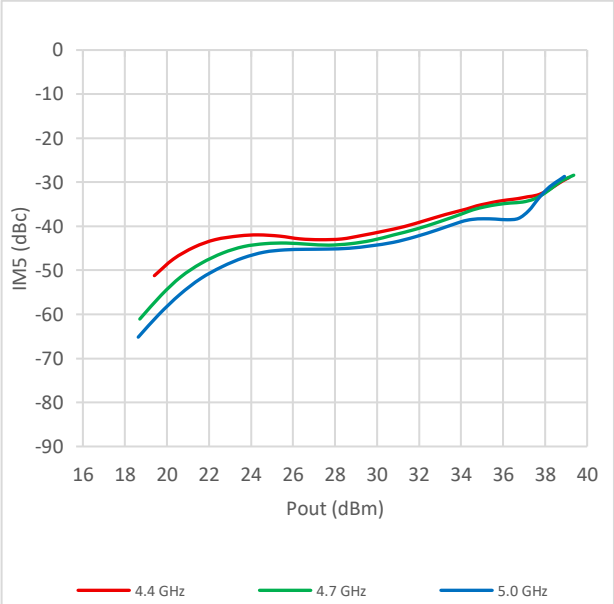


Figure 25 - IMD5 vs Pout

Test conditions unless otherwise noted
Vd = 28 V, Idq = 56mA, Ta = + 25 °C, Zo = 50 Ω.

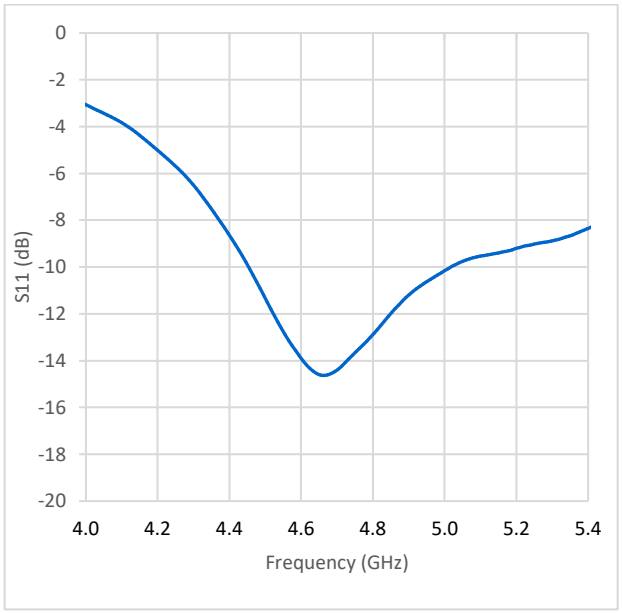


Figure 26 - Input Return Loss, S11

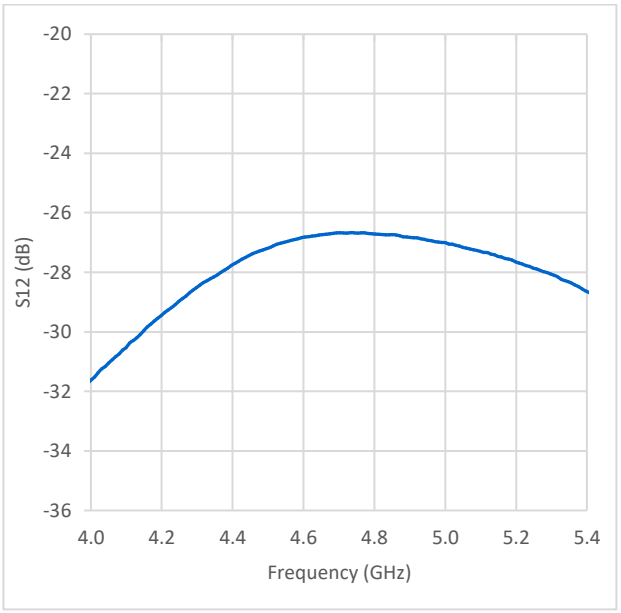


Figure 27 - Reverse Isolation, S12

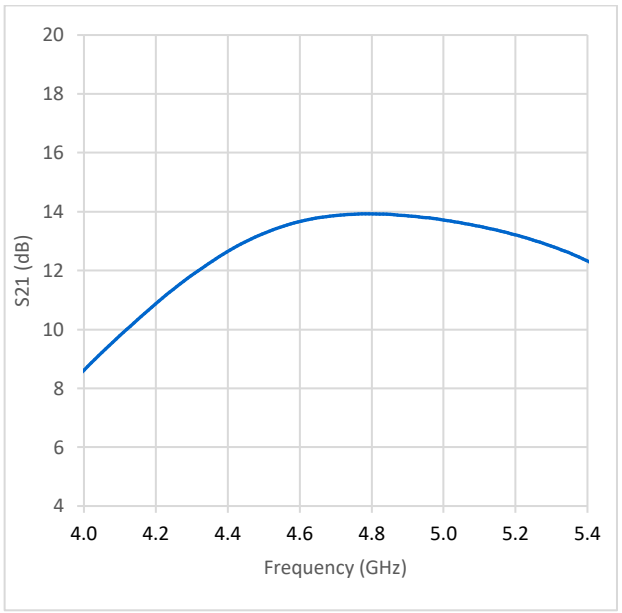


Figure 28 - Small Signal Gain, S21

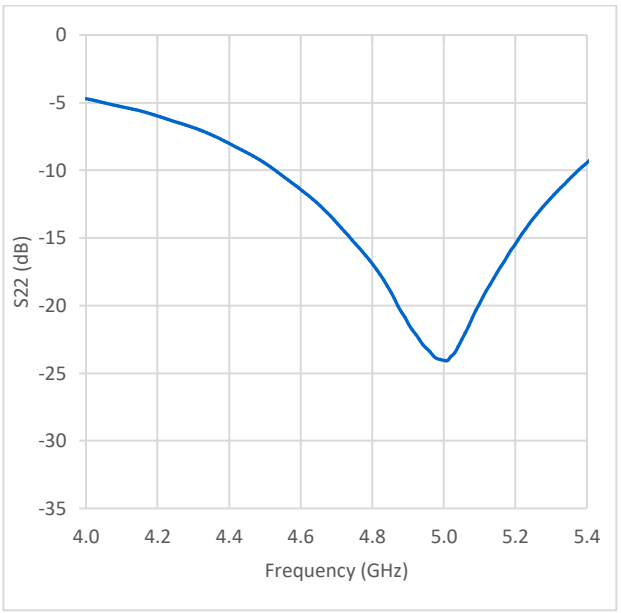


Figure 29 - Output Return Loss, S22

Test conditions unless otherwise noted
Vd = 28 V, Idq = 56mA, over varying temperature, Zo = 50 Ω.

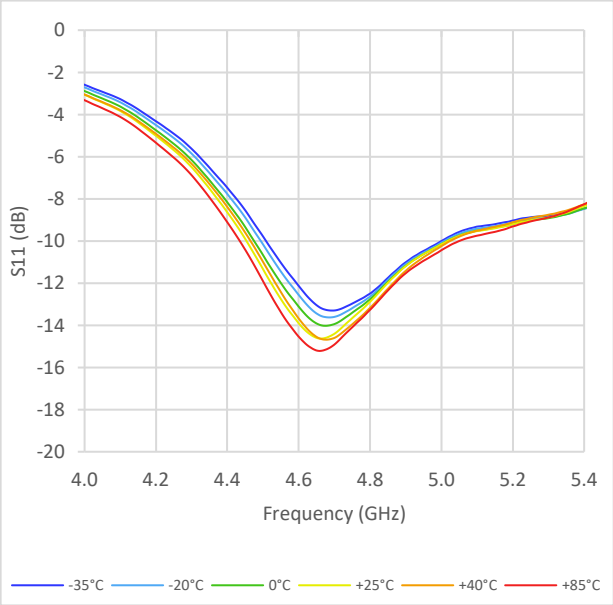


Figure 30 - Input Return Loss, S11

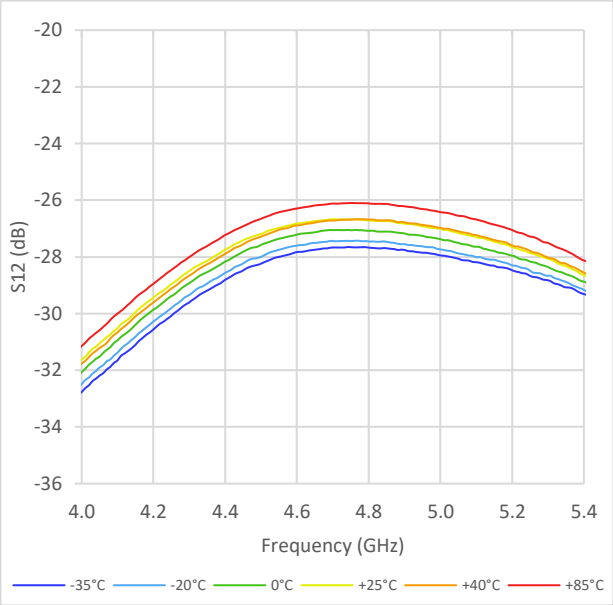


Figure 31 - Reverse Isolation, S12

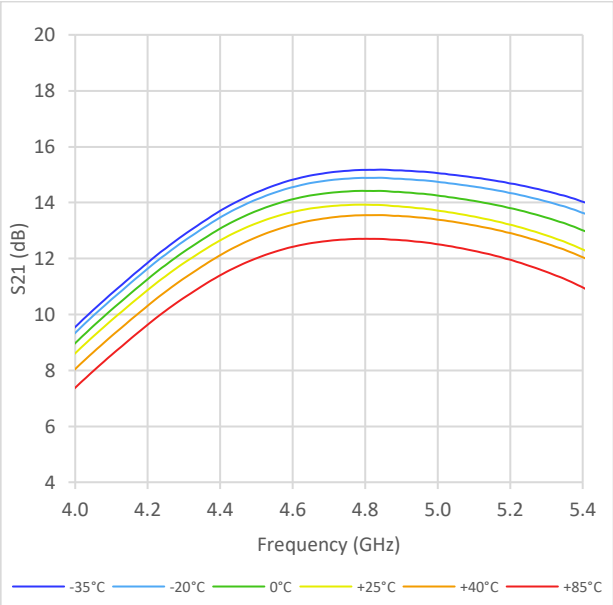


Figure 32 - Small Signal Gain, S21

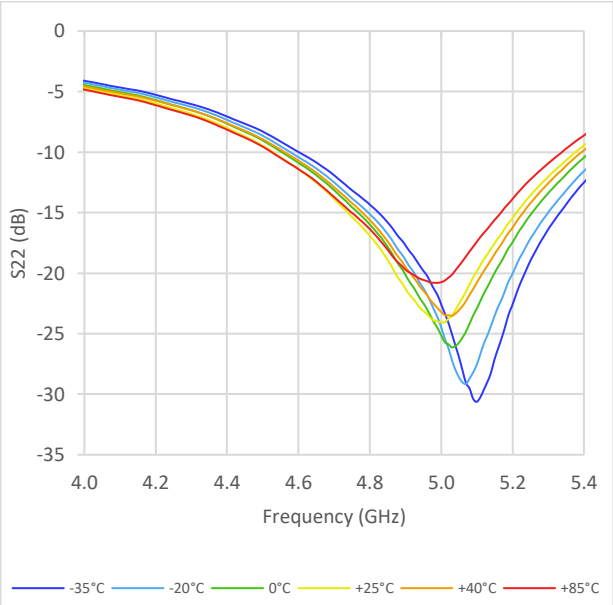


Figure 33 - Output Return Loss, S22

Test conditions unless otherwise noted
Vd = 28 V, Idq = 56mA, Ta = +25 °C, Zo = 50 Ω.

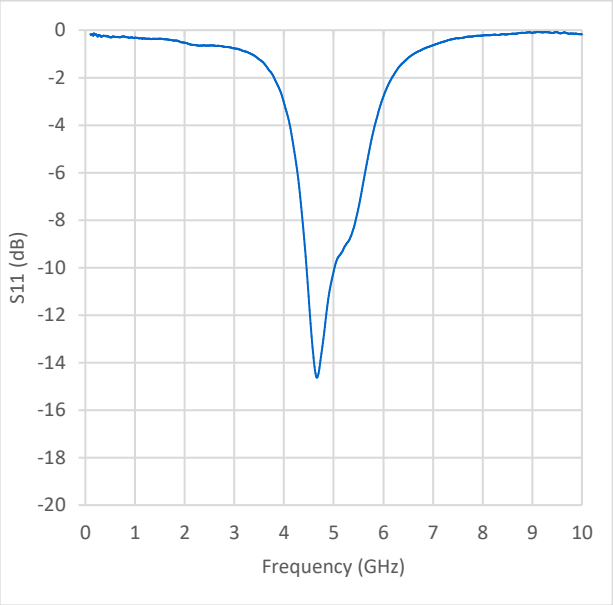


Figure 34 - Input Return Loss, S11

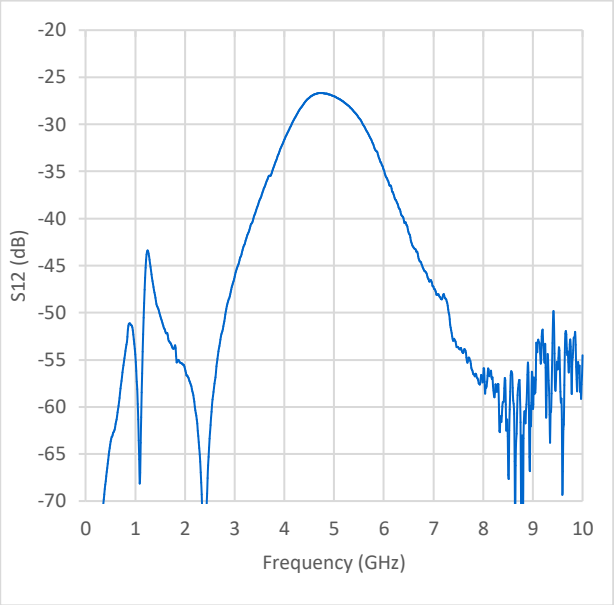


Figure 35 - Reverse Isolation, S12

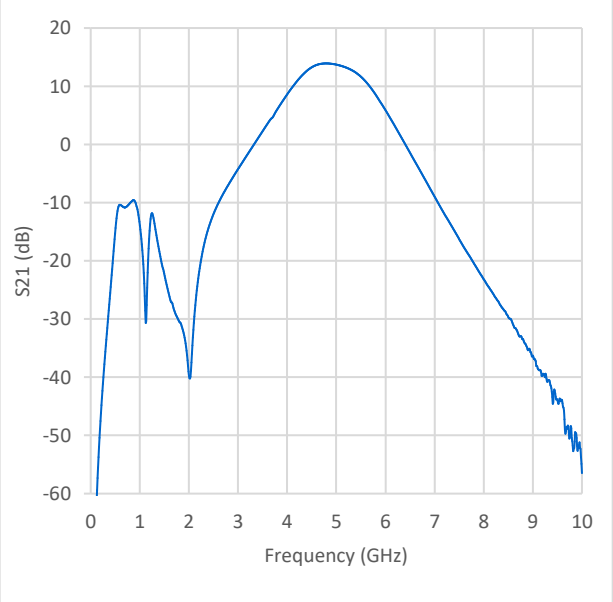


Figure 36 - Small Signal Gain, S21

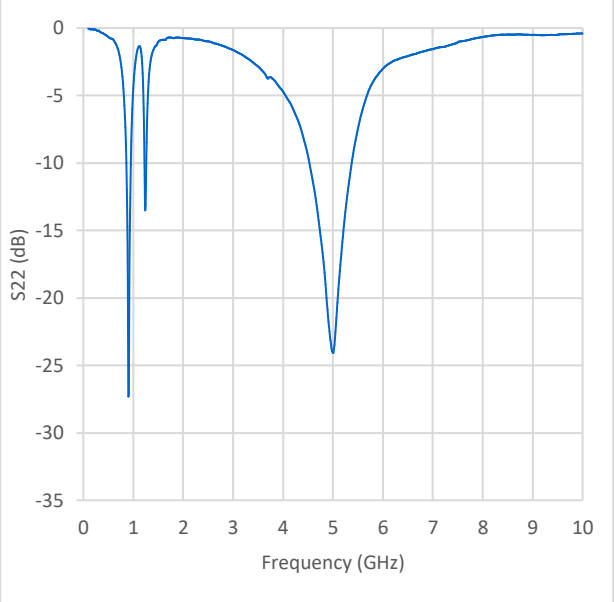


Figure 37 - Output Return Loss, S22

Test conditions unless otherwise noted
Vd = 28 V, Idq = 56mA, over varying temperature, Zo = 50 Ω.

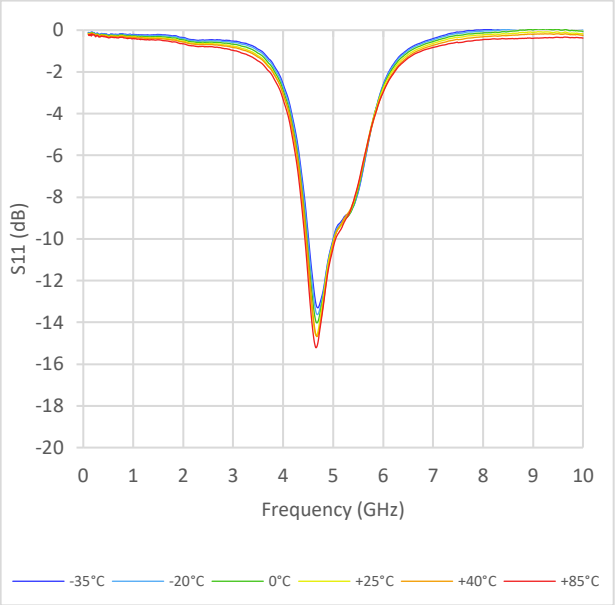


Figure 38 - Input Return Loss, S11

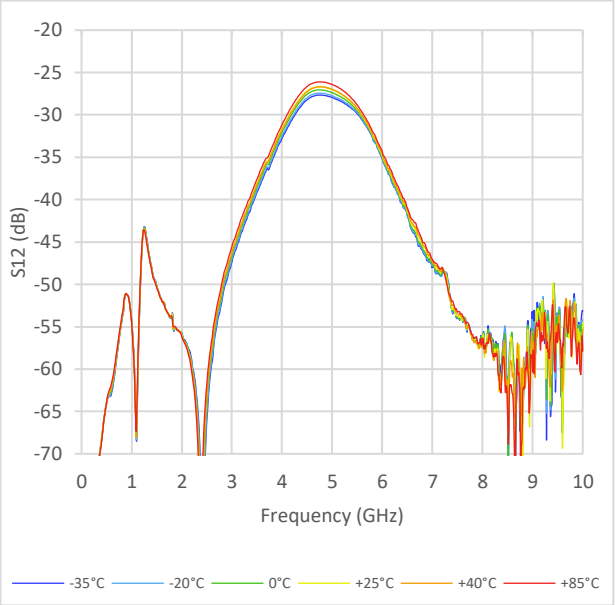


Figure 39 - Reverse Isolation, S12

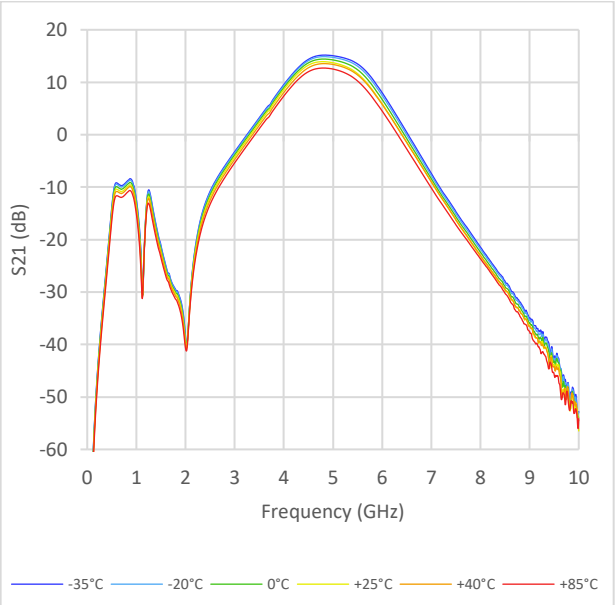


Figure 40 - Small Signal Gain, S21

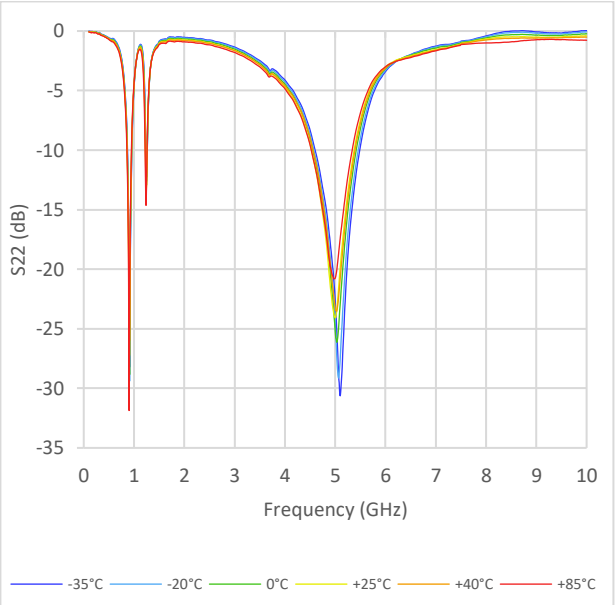


Figure 41 - Output Return Loss, S22

Application Information

IMPORTANT: Bias Procedure

The MGX-445040-S5 device is depletion mode and requires the (negative) gate bias to be applied before the (positive) drain bias, otherwise damage may occur.

Bias sequence:

1. Set Vgs voltage to -4.5 V (pinched-off)
2. Set Vds voltage to required value (28 V)
3. Set Vgs to give Ids = 56 mA (~-2.4 V) with no RF applied

Schematic Diagram

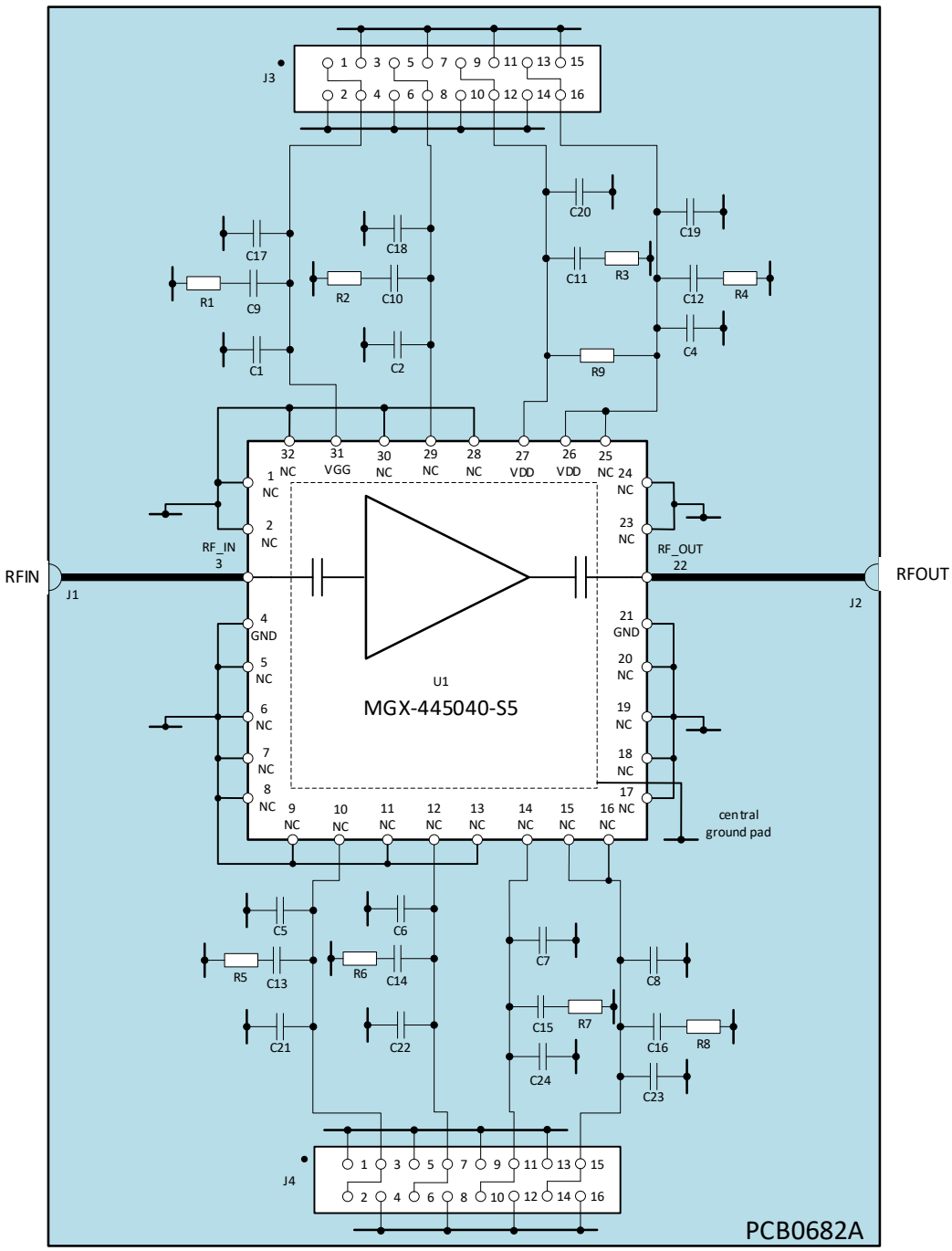


Figure 42 - MGX-445040-S5EV Schematic

Bill of Materials

Table 2 - Bill of Materials

Reference Designator	Value	Size	Description
C1, C4	10 nF	0402	X7R, 50V, ±10 %
C9, C12	1 µF	0603	X7R, 50V, ±10 %
C17, C19	10 µF	1206	X7R, 50V, ±10 %
R1, R4	4.7 Ω	0603	0.1 W, ±1 %
R9	0 Ω	0402	0.063W, ±1 %
U1	MGX-445040-S5		
J1, J2	Mueller Electric Co, RF Connector, SMA edge mount, BU-1420701841		
J3	Samtec, SMD, 0.1”, 16-way header, IPL1-108-02-L-D-K		
C2, C5, C6, C7, C8, C10, C11, C13, C14, C15, C16, C18, C20, C21, C22, C23, C24, R2, R3, R5, R6, R7, R8, J4	DNF	-	

Notes

- DNF = Do not fit component

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number MGX-445040-S5EV).

The PCB is a multi-layer PCB, with ENIG metal finish and all SMT components mounted on the top side. For optimal performance all RF PCB structures are referenced layer 1 to 2 with Rogers RO4350B core, 10 thou thickness with 0.5 oz copper. The inner layer is standard FR4 core for rigidity (Figure 43). The PCB is then mounted to an aluminium carrier, 6 mm thick, to provided thermal dissipation. The MGX-445040-S5EV (PCB0682A - Figure 44), is 38 mm x 54 mm.

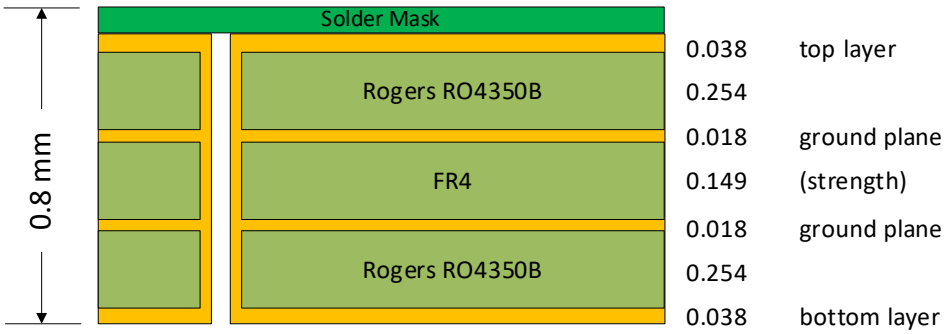


Figure 43 - MGX-445040-S5EV (PCB0682A) Layer Stack

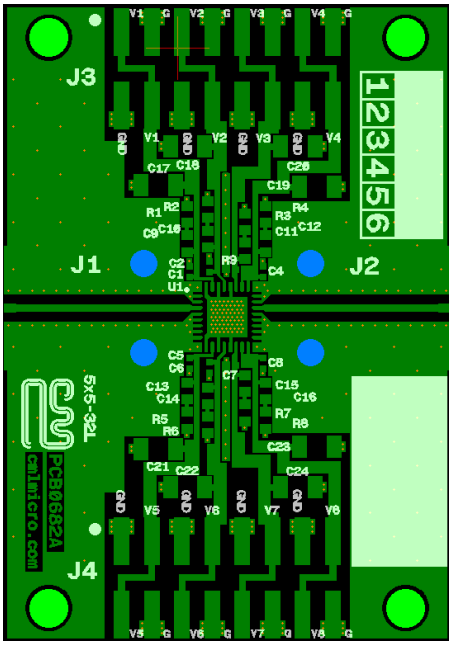


Figure 44 - MGX-445040-S5EV PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed ground pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. MGX-445040-S5EV has 72 x 0.2 mm, resin filled grounding vias connecting the top layer all other layers in the ground central pad area.

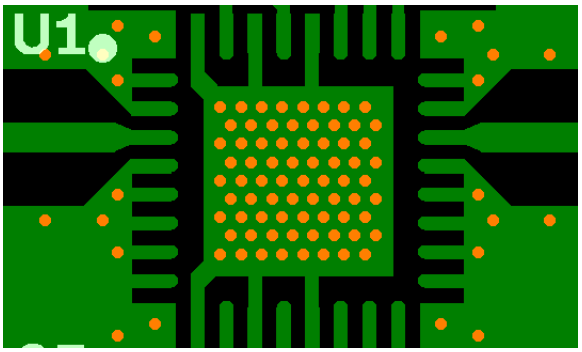


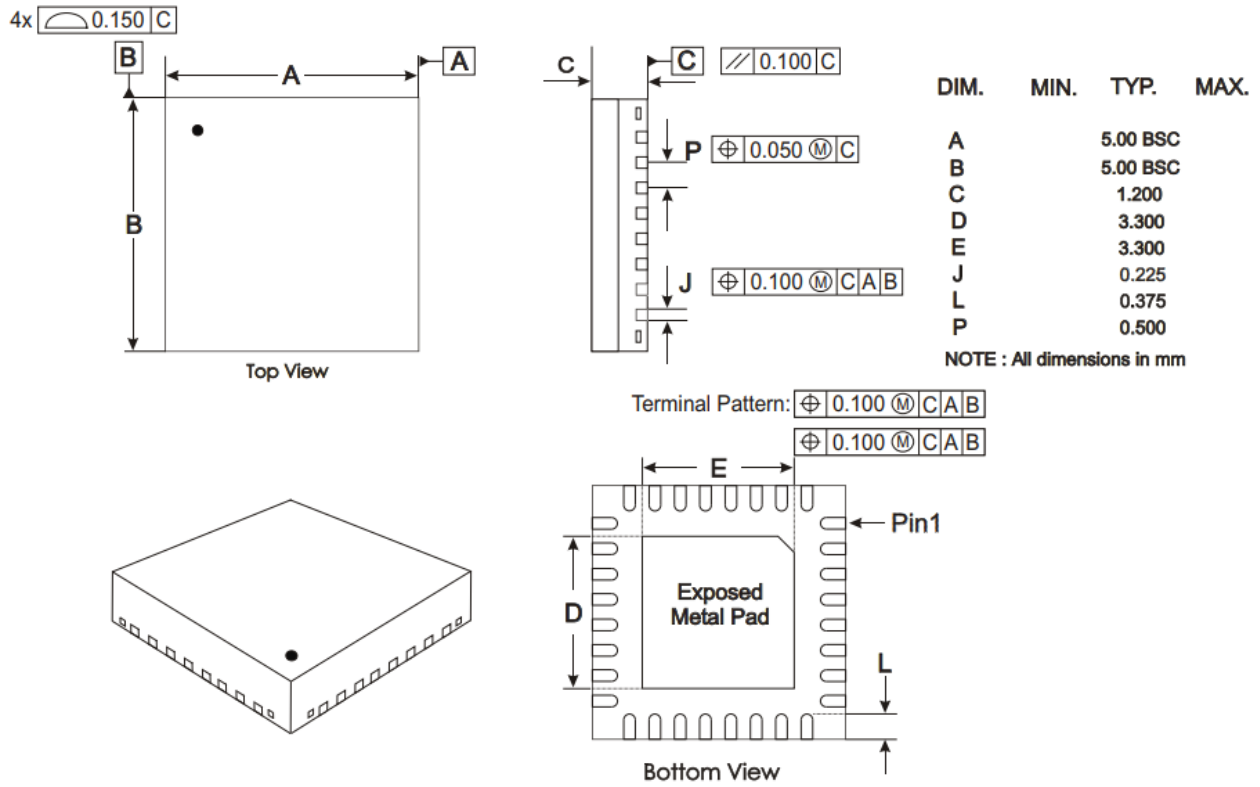
Figure 45 - MGX-445040-S5EV Ground Vias

The device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin – Pout and Tc is the case temperature on the backside of the package (central ground pad) in contact with the PCB.

The four mounting holes in the MGX-445040-S5EV near U1 (blue circles in Figure 44) should be used to mount the PCB on to the aluminium carrier using M2 screws. The MGX-445040-S5EV PCB plus carrier can then be mounted to a larger heatsink using the four mounting holes in the corners of the board using M3 screws.

Package Outline

32-lead 5 x 5 mm AQFN Package (S5)



The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 46 - Package Outline

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: Product Range Identifier

Line 2: 6-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1	First public release	October 2026

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